A New Methodology for the Computation of the Substrate Parasitics of Octagonal Inductors

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Abstract — **The paper provides a method for the computation of the substrate parasitics of symmetrical octagonal inductor., using a set of equivalent structures. This method has been tested on a wide range of inductors and the error due to computation is lower than the one due to the topology of the model itself.**

I. INTRODUCTION

Most of the inductor models focus on the serial part of the devices (inductance, series resistance, overlap capacitance), and scaleable models are available for these elements [1][2][3]. In the opposite, very few authors take care about an accurate modelling of the oxide and substrate behavior. Though, the errors done on the substrate modelling have an influence on the quality factor and the self-resonant frequency.

The inductors considered here are symmetrical multi-level, octagonal and protected by a grounded ring. A study of all the coupling effects between each track and the ground would take a big amount of resources and time (CPU, memory). On the other hand, a succession of approximations (parallel-plate capacitors) often leads to huge errors in the model.

In this paper, we propose a simple and accurate method to compute the oxide and silicon capacitances and the silicon resistance. This method is based on the definition of several equivalent structures for the computation of these parasitics. The results obtain are fully scaleable according all the inductance characteristics (Fig. 1) : number of turns, spacing, width, diameter, metal and oxide thickness, substrate resistivity.

II. DESCRIPTION OF THE EQUIVALENT STRUCTURES

A typical on-chip inductor is composed of several metal layers in parallel connected to each other with vias. To simplify the computation of the oxide capacitance, we use an equivalent structure where the metal layers are stacked together (Fig.2), the total thickness of the metal (Tmeteq) is equal to the sum of all the layer thickness. Then, we can

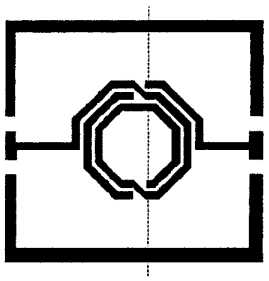

Fig. 1.a : Layout of an inductor

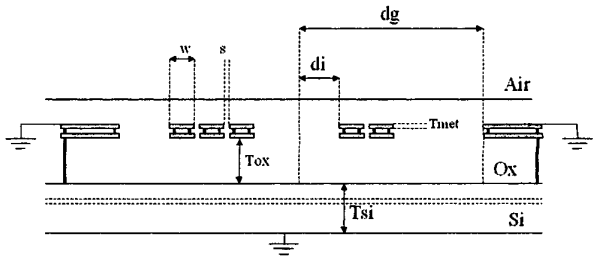

Fig. 1.b : Cross section on an inductor.

apply the strip line formalism.

The determination of the substrate capacitance is done by using another structure (fig. 3). In the same way as previously, the metal layers are put together and on top of that the space between the inner and outer turn of the inductor is filled with metal. As a result we get a ring composed of two parts with different widths, due to the asymmetry of the inductor. To validate the assumption concerning this structure, we ran electromagnetic simulations with Momentum and we compared the substrate admittances of the inductor and the equivalent structure (Fig. 4). We see a good agreement between these simulations.

For the evaluation of the capacitance we must consider separately the two half rings. The total width of the final central track is equal to twice the width of the ring, then, the computed capacitance is divided by two. In this way,

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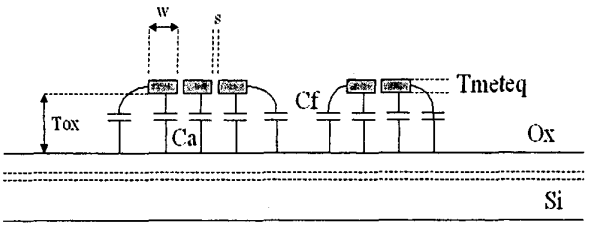

we Fig. 2 Equivalent structure for the computation of the oxide capacitance.

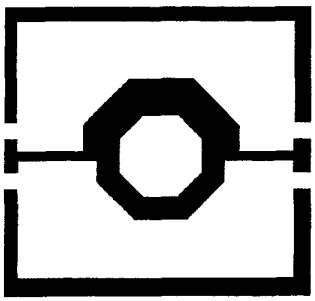

Fig. 3 : Equivalent ring for the computation of the substrate capacitance.

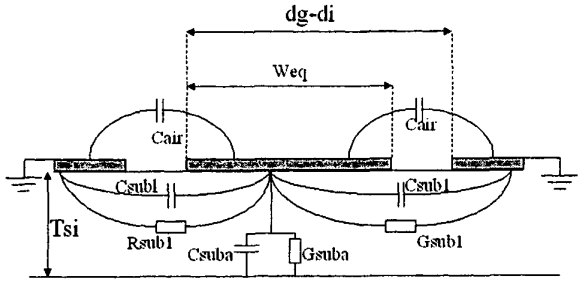

Fig 4. Equivalent structure for the computation of the substrate capacitance.

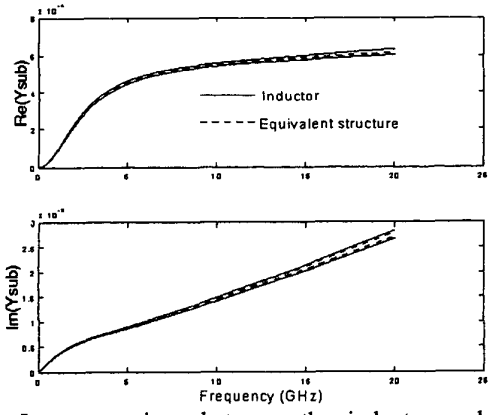

Fig. 5 : comparison between the inductor and the equivalent ring substrate admittance.

can approximate the coupling of the tracks with the closest ground plane and neglect the coupling with the other ground plane.

III. PARAMETERS COMPUTATION

According to Fig. 2, the oxide capacitance Cox is the sum of a parallel plate capacitance Ca and a fringing capacitance Cf.

Ca can be calculated very simply

$$C_a = \frac{\varepsilon_0 \varepsilon_{ox} W l}{t_{ox}} \tag{1}$$

where W is the width of the track of an inductor and l the total length of the inductor, including the access.

Cf is computed with an empirical formula described in [4] :

$$C_f = 2.8\varepsilon_0 \varepsilon_{ox}(p_{in} + p_{out})\left(\frac{t_{meteq}}{t_{ox}}\right)^{0.222} \tag{2}$$

Where pin and pout are the inner and outer perimeters of the inductance.

For the computation of the substrate capacitance, we use a quasi-static approach applied to coplanar lines [5].

The equivalent structure is twice larger as the total width of the inductor, so the computed capacitance will have to be divided by two. According to the quasi-static evaluation of a distributed capacitance based on the Schwartz-Cristoffel transform, the substrate capacitance Csub per unit length can be expressed as

$$C_{sub} = \varepsilon_0 \varepsilon_{sub} \frac{K(k_{sub})}{K(k'_{sub})} \tag{3}$$

with

$$k_{sub} = \frac{\tanh\left(\frac{\pi W_{eq}}{2t_{si}}\right)}{\tanh\left(\frac{\pi(d_g - d_i)}{2t_{si}}\right)} \tag{4}$$

$$k'_{sub} = \sqrt{1 - k_{sub}^2} \tag{5}$$

K(k) is the elliptic integral of k, dg and di are the distance of the lateral ground plane to the center of the inductor and the internal radius.

In the same way, we can have the air capacitance Cair, replacing ksub by

Dout	N	W	Cox meas (fF)	Cox calc (fF)	Csub meas (fF)	Csub calc (fF)	Rsub meas (ohm)	Rsub calc (ohm)	Cair calc (fF)	delta(Cox) (%)	delta(Csub) (%)	delta(Rsub) (%)
156	2	10	198	196	53	41	141	166	2	1,0	22,6	-17,7
168	2	15	254	258	49	45	150	147	2	-1,6	8,2	2,0
200	2	20	332	334	56	51	126	129	3	-0,6	7,3	-2,4
200	3	15	353	352	50	51	128	129	3	0,3	-2,0	-0,8
232	4	15	483	466	59	59	126	129	4	3,5	0,0	-2,4
242	3	20	486	478	62	61	119	109	4	1,6	1,6	8,4
244	6	10	558	500	70	62	118	111	4	10,4	11,4	5,9
288	8	10	722	709	86	73	92	93	5	1,8	15,1	-1,1

Table 1 : Comparison between the measured and computed values of the substrate components.

$$k_{air} = \frac{W_{eq}}{d_g - d_i} \qquad (6)$$

Finally, given the silicon resistivity ρsub, the substrate conductance per unit length is equal to [6][7]

$$G_{sub} = \frac{C_{sub}}{\varepsilon_0 \varepsilon_{ox} \rho_{sub}} \qquad (7)$$

III. Results

The table 1 summarizes the results obtained on a set of inductors processed in CMOS 0.25um technology. The number of turns varies from 2 to 8 and the width from 10 to 20 um. In most cases, the error on each parameter is lower than ten percents, and even better for 'medium-size' inductors.

We did a comparison between the measurements of inductors and the models ; a tuned model [8] and another one with the same topology but the substrate parasitics are replaced by the new ones (Fig. 6).

We can see that thanks to a very accurate computation of the oxide capacitance, the errors done on the substrate capacitance and resistance play a minor role on the substrate admittance, at least until 20GHz. These inaccuracies do not affect much the transmission impedance of the inductor neither. The error related to the topology of model itself is more important than the error caused by the inaccuracy of the capacitor computation.

IV. Conclusion

In this paper, we presented a new method for the computation of the oxide and silicon capacitances and resistance for octagonal inductors. This method is based on

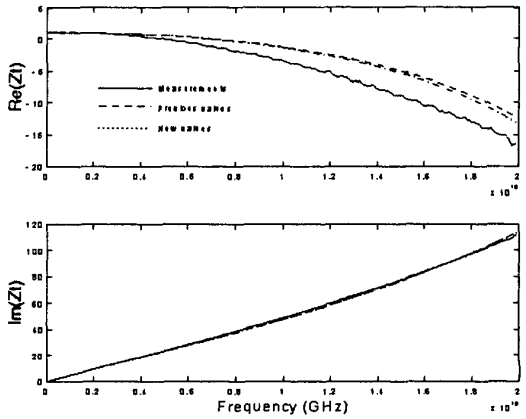

Fig. 6.a Comparison of the transmission impedances

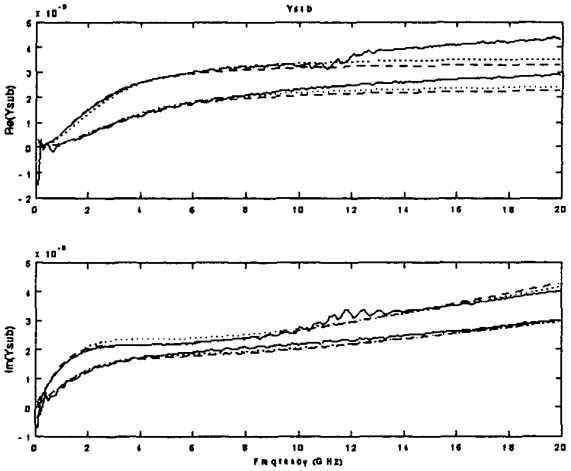

Fig. 6.b Comparison of the substrate admittance

the analysis of equivalent structures having the same substrate admittance as the inductor itself. Then, transmission lines theory is used to evaluate the substrate parasitics. The results are accurate in spite of simplicity of the equivalent structures and the computations can easily be implemented in applications such as a fully scaleable inductor model.

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